Scientific Paper / Artículo Científico

UNIVERSIDAD POLITÉCNICA SALESIANA ECUADOR
INGENIUS
Revista de Ciencia y Tecnología
https://doi.org/10.17163/ings.n24.2020.07
pISSN: 1390-650X / eISSN: 1390-860X

Control for the output voltage on a flying capacitor multilevel inverter

Control para el voltaje de salida de un inversor multinivel de capacitores flotantes

Beatriz Angélica Aguilar-López[1], José Antonio Juárez-Abad[2,*], Jorge Luis Barahona-Avalos[2], Rosalino Mayoral-Lagunes[1], Jesús Linares-Flores[2], Marco Antonio Contreras-Ordaz[2]

Abstract

This paper presents the design of a robust Active Disturbance Rejection Controller (ADRC) for tracking the reference trajectory of the output voltage of a flying capacitor multilevel inverter. If the dynamics of each flying capacitor and of the passive elements of the filter are considered in the dynamic model of the converter, it results a high order model, which is difficult to control. PS-PWM modulation is used in this work to keep the voltages in the flying capacitors at their nominal values, and thereby generate a second-order simple dynamic model that is easier to control. The simulation and experimental results confirm that the controller is robust in the presence of disturbances, caused by either linear or nonlinear load changes. The experimental prototype of the complete system was built, and the implementation of the controller and the modulator was carried out in a FPGA; the results obtained are shown in the final part.

Keywords: Active Disturbance Rejection, Exact Linearization, Flying Capacitors, Natural balancing, Power converter, Robust Control.

Resumen

Este artículo presenta el diseño de un controlador mediante la técnica de rechazo activo de perturbaciones para el seguimiento de la trayectoria de referencia para el voltaje de salida de un inversor multinivel de capacitores flotantes. Si en el modelo dinámico del convertidor se consideran las dinámicas de cada capacitor flotante, adicionalmente, las de los elementos pasivos del filtro de salida, el modelo resultante es de un orden alto, lo que dificulta su control. En este trabajo se emplea la modulación PS-PWM para mantener los voltajes en los capacitores flotantes en sus valores nominales y de esta manera poder generar un modelo dinámico simple, que resulta ser más fácil de controlar. Los resultados de simulación y experimentales, confirman que el controlador es robusto a perturbaciones provocadas por cambios en la carga, sin importar si son de tipo lineal o no lineal. Se realizó la construcción del prototipo experimental del sistema y se implementó el controlador y modulador en un FPGA y en la parte final se muestran los resultados obtenidos.

Palabras clave: balanceo natural, capacitores flotantes, control robusto, convertidor de potencia, linealización exacta, rechazo activo de perturbaciones.

[1]División de estudios de posgrado, Universidad Tecnológica de la Mixteca - México.
http://orcid.org/0000-0002-2769-4992, http://orcid.org/0000-0003-3420-7416
[2,*]Instituto de Electrónica y Mecatrónica, Universidad Tecnológica de la Mixteca - México.
Corresponding author ✉: abad@mixteco.utm.mx
http://orcid.org/0000-0001-7440-0849, http://orcid.org/0000-0002-5502-6692
http://orcid.org/0000-0002-5723-4786, http://orcid.org/0000-0002-3478-796X

Received: 22-11-2019, accepted after review: 03-06-2020

Suggested citation: Aguilar-López, B. A.; Juárez-Abad, J. A.; Barahona-Avalos, J. L.; Mayoral-Lagunes, R.; Linares-Flores, J. and Contreras-Ordaz, M. A. (2020). «Control for the output voltage on a flying capacitor multilevel inverter». Ingenius. N.° 24, (july-december). pp. 68-80. doi: https://doi.org/10.17163/ings.n24.2020.07.

1. Introduction

Electric power may be available in two modes: direct current (DC) or alternating current (AC). There are applications where it is required the transformation from one mode to the other, and such conversion is carried out by a device known as power converter; for example, the AC-DC transformation is performed by a converter called rectifier, and the DC-AC conversion is carried out by a converter called inverter [1]. The power converters are built with commutation devices and passive elements such as capacitors, inductors, diodes and transformers. In general, the power that the converter is capable of delivering is limited by the current and voltage ratings of its switches and commutation devices.

Even though an inverter should ideally produce a sinusoidal voltage in traditional applications of alternating current (to achieve better efficiency and low electromagnetic interference, among other advantages [2]), they are only capable of producing rectangular waves (i.e., with three levels). With the rise of multilevel inverter topologies, it was possible to generate voltage waves with multiple levels, which are more similar to the ideal sinusoidal wave. The most well-known topologies of multilevel converters are: cascade cells, diode clamped and flying capacitor [3]. The first topology mentioned consists of a series connection of H-bridges and requires isolated voltage sources for each of the cells, while the last two require only one voltage source [4].

The topology of flying capacitor multilevel converters (FCMC) has demonstrated to be an excellent choice in applications where high power density is required [5]. The structure of a FCMC consists of power cells. Each power cell is constituted by a pair of switches and a flying capacitor. The number of levels at the output of the FCMC may be increased by adding more cells to the FCMC, but more capacitors and switches are required. Each flying capacitor should be charged to a particular nominal voltage. Depending on the state of the cell switches, the flying capacitor will or will not supply its voltage at the output of the converter.

For the correct operation of the FCMC, a balanced distribution in the voltages of the flying capacitors should be maintained: each of them should maintain a nominal voltage equivalent to a fraction of the total voltage of the DC bus divided between the number of cells. Two independent processes known as precharge and balancing (or regulation) of the voltages in the flying capacitors, are carried out to achieve a correct operation of the FCMC.

For the case of the precharge, some reported methods may be found in [6] and [7]. On the other hand, the balancing of the voltages in the flying capacitors may be carried out passively and actively. The natural or passive balancing utilizes a modulation technique commonly called Phase Shifted-PWM (PS-PWM). This modulation technique is employed to generate the commutation states that form the desired output voltage signal and, at the same time, it maintains an average net charge equal to zero in the flying capacitors.

The aforementioned passive balancing technique is easy to implement, but it does not guarantee that the voltages of the capacitors reach their nominal values, because the components utilized in the construction of the FCMC regularly have non-ideal conditions, i.e.: unequal leakage currents in the capacitors, asymmetrical charge and discharge in the capacitors and load disturbances, among others [8]. On the other hand, in active balancing the voltage of the flying capacitors is individually regulated. This approach requires the use of a voltage sensor for each of the flying capacitors as shown in [9] and [10], or estimating them by means of observers as it is considered in [11].

A necessary control task in power converters is supplying an output voltage of constant amplitude, regardless of the effective load resistance. For the case of the DC-AC converter it is desired that the output tracks a reference voltage despite the disturbances that occur due to changes in the load current or in the input voltage [12]. A feedback control system is required for these tasks to be carried out precisely. Voltage tracking in multilevel inverters has been addressed using different control techniques. Different control schemes have been employed for the cascade cells topology, which include: passivity-based controller [13] and generalized proportional integral tracking control [14]. Voltage tracking for the flying capacitor topology has been carried out in [15] and [16]. In [15], each appropriate commutation state is generated to produce the desired output voltage, using an algorithm that does not require an additional modulation nor the model of the converter. In [16], the authors state that the tasks of voltage balancing and voltage reference tracking are coupled, which becomes a serious problem in high bandwidth and high precision applications. They emphasize in the decoupling of these tasks by means of two techniques: feedback linearization and a variant of vector space modulation. Proportional-integral (PI) and linear quadratic regulator (LQR) controllers are applied for voltage tracking, and simple proportional (P) controllers for balancing the voltages in the capacitors.

The objective of the present work is the tracking control of a sinusoidal reference signal applied to the output voltage of a FCMC. The PS-PWM modulation is responsible for the task of balancing the voltages in the flying capacitors. This enables avoiding the use of multiple voltage sensors, and reducing the complexity of both the converter dynamic model and of the controller implementation. The controller is based on the Active Disturbance Rejection Control (ADRC) technique.

Section 2.1 describes the components of the system: controller, modulator and power converter. The average dynamic model of the FCMC is obtained in section 2.2. The exact linearization of the FCMC model is carried out in section 2.3. The design of the ADRC-based controller is presented in section 2.4. Section 3 shows the results of the cosimulation carried out in Matlab-Simulink/PSIM, where it is analyzed the effectiveness of the controller before the experimental construction, the experimental results are shown in section 4 and, at last, the conclusions are presented in section 5.

2. Materials and methods

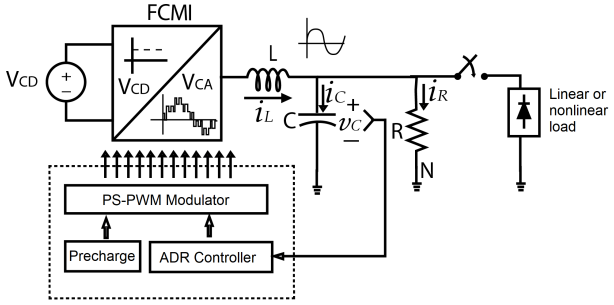


Figure 1. Block diagram of the system.

Figure 1 shows the complete system which is described in the following. From a direct current voltage source, V_{CD}, the FCMC synthetizes at the output a signal with multiple voltage levels based on PWM. Such output voltage is processed by a low pass LC passive filter, with the purpose of attenuating the high frequency components of the PWM signal and, at last, obtaining a voltage signal purely sinusoidal at the output of the filter. The active disturbance rejection controller feedbacks the voltage signal of the filter and compares it against a sinusoidal reference signal, of frequency 60 Hz and variable amplitude; the reference or modulating signal is employed for the PS-PWM modulator. During the firing of the FCMC the flying capacitors are discharged, and therefore, the correct voltage, or nominal voltage, in each of them is established by means of the precharge process.

Initially, a resistive load with known value is connected in parallel with the capacitor C of the output filter, and at a given time a linear or nonlinear load is added to the system as an external disturbance.

The FCMC is shown in Figure 2, which consists of multiple power cells connected one after another. Each power cell (except the one connected to the DC bus) contains a pair of power switches and a flying capacitor.

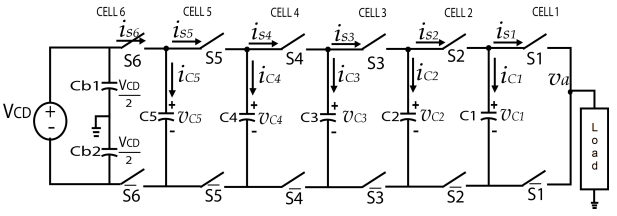


Figure 2. Topology of the flying capacitor multilevel inverter (FCMI).

For example, cell 1 is constituted by switches $S1$, $\bar{S1}$ and by capacitor $C1$. Six cells are required to obtain seven voltage levels, including the level corresponding to $0V$. Each flying capacitor of the ith cell, should be charged and should be maintained at a nominal voltage V_{Ci}, which may correspond to any of the following values: $V_{CD}/6$, $2V_{CD}/6$, $3V_{CD}/6$, $4V_{CD}/6$, $5V_{CD}/6$.

Individually, each switch of the converter may be closed (ON) or open (OFF). For the purpose of avoiding short circuits in the cells, the switches of each cell should operate in a complementary manner, and consequently never should remain closed at the same time; this condition is guaranteed using a delay time between commutations. In the flying capacitors topology, as well as in other multilevel topologies, a particular level of voltage may be obtained with different commutation states, which are called redundant states. In the topology of half-bridge FCMC of seven levels, the following voltage levels may be obtained at the output: $-3V_{CD}/6$, $-2V_{CD}/6$, $-V_{CD}/6$, 0, $V_{CD}/6$, $2V_{CD}/6$, $3V_{CD}/6$.

2.1. Average dynamic model

Applying Kirchhoff's current law to the FCMC shown in Figure 2, the following set of equations for the currents in the flying capacitors is obtained:

$$\begin{aligned} C_1\frac{dv_{C1}}{dt} &= i_L(d_2-d_1)\\ C_2\frac{dv_{C2}}{dt} &= i_L(d_3-d_2)\\ C_3\frac{dv_{C3}}{dt} &= i_L(d_4-d_3)\\ C_4\frac{dv_{C4}}{dt} &= i_L(d_5-d_4)\\ C_5\frac{dv_{C5}}{dt} &= i_L(d_6-d_5) \end{aligned} \tag{1}$$

where i_L is the current through the inductor of the output filter, C_i is the capacitance of the capacitors of the FCMC, d_i represents the duty cycle of the S_i switch and v_{Ci} are the voltages in the flying capacitors, with $i = \{1, 2, 3, 4, 5\}$.

The output voltage of the FCMC of Figure 2 is measured from node va with respect to ground and is called v_{aN}„ which is determined in the following manner:

$$v_{aN} = v_{C1}(d_1 - d_2) + v_{C2}(d_2 - d_3) + v_{C3}(d_3 - d_4) + v_{C4}(d_4 - d_5) + v_{C5}(d_5 - d_6) + V_{CD}d_6 - \frac{V_{CD}}{2} \quad (2)$$

The PS-PWM modulation generates the PWM signals for each pair of switches of the cells of the FCMC. Figure 3(a) shows some cycles of the carrier signals $C1$ to $C6$, which are triangular signals with amplitudes that take values in the interval $[-1, 1]$ and frequency f_c, 60 degrees out of phase. The frequency of the carriers is greater than the frequency f_m of the modulating signal, and consequently it is common to define a modulating index $\frac{f_c}{f_m} \geq i_m$. In this work, a modulating index $i_m = 40$ was employed. For the case of the modulating signal u_{av}, its amplitude takes values in the interval $[-1, 1]$ and has a frequency $f_m = 60\ Hz$.

Each carrier signal is compared with the modulating signal to obtain the PWM signals, as can be seen in Figure 3(b), producing the PWM signals named as $V_a - V_f$, which have the same duty cycle d.

Applying this signal to the FCMC of seven levels, all switches have the same duty cycle, i.e.:

$$d_1 = d_2 = d_3 = d_4 = d_5 = d_6 = d \quad (3)$$

According to equation (1), the variation of the average voltage in each flying capacitor is zero when all duty cycles, d_1 to d_6, are equal. Therefore, the dynamics of the voltages (1) in the flying capacitors can be considered as constant, and their derivatives equal to zero. This is the reason why the dynamics of the capacitors may not be considered in the average model of the FCMC.

On the other hand, there is a relationship between the duty cycle d and the modulating signal u_{av}, which is expressed as $d = \frac{u_{av}}{2} + 0.5$. Considering this and substituting (3) in (2), the output voltage V_{aN} can be expressed as follows:

$$v_{aN} = V_{CD}(d) - \frac{V_{CD}}{2} = \frac{V_{CD}}{2}u_{av} = Eu_{av} \quad (4)$$

where E is the voltage of each of the capacitors $Cb1$ and $Cb2$, whose value is $V_{DC}/2$. Equation (4) enables seeing the FCMC of seven levels in a simplified manner, as a multilevel converter «reducer» with a supply voltage source Eu_{av} (where $E = V_{CD}/2$), a low pass LC filter and a varying load, as shown in Figure 4.

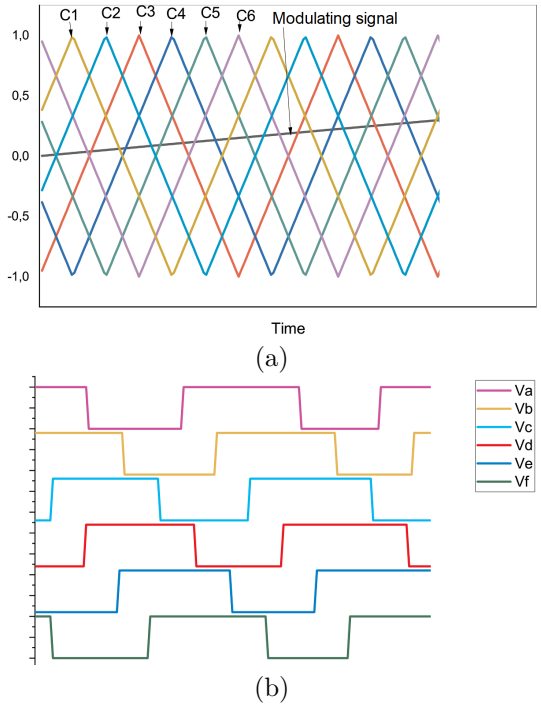


Figure 3. PS-PWM modulation: (a) Carriers of the modulation; (b) Duty cycle in the generated PWM channels.

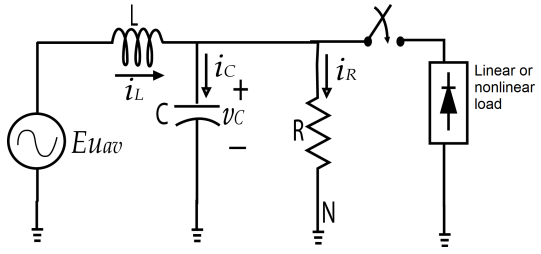


Figure 4. Simplified model of the flying capacitor multilevel inverter.

Considering the above, the second order average model of the FCMC can be expressed as in (5):

$$L\frac{di_L}{dt} = -v_C + Eu_{av}$$
$$C\frac{dv_C}{dt} = i_L - \frac{v_C}{R} \quad (5)$$

The control input u_{av} represents the PWM modulating signal, which can take values in the continuous interval $[-1, 1]$. The term v_C is the voltage in the filter capacitor. The current that circulates through the switches and through the output inductance is i_L, L and C are the values of the inductance and capacitance of the filter, respectively.

2.2. Exact linearization of the model

The FCMC system previously described is linear, Single Input-Single Output (SISO) and, as it was men-

tioned above, of reducing nature. Regrouping the model shown in equation (5) to be expressed in its nonlinear affine form, yields:

$$\begin{aligned} \dot{x} &= f(x) + g(x)u \\ y &= h(x) \end{aligned} \tag{6}$$

where:

$$f(x) = \begin{pmatrix} -\frac{v_C}{L} \\ \frac{i_L}{C} - \frac{v_C}{RC} \end{pmatrix}, \quad g(x) = \begin{pmatrix} \frac{E}{L} \\ 0 \end{pmatrix}$$

and:

$$x = \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} = \begin{pmatrix} i_L \\ v_C \end{pmatrix}$$

As it is widely described in [17], the output function that enables exact linearization of the nonlinear system (6) is given as:

$$h(x) = v_C \tag{7}$$

The relative degree r of the nonlinear system (6) is obtained by means of the successive calculation of the Lie derivatives:

$$L_g L_f^k h(x) = 0 \tag{8}$$

until finding the Lie derivative that satisfies:

$$L_g L_f^{r-1} h(x) \neq 0 \tag{9}$$

where $k < r-1, \forall x \in \Omega$. The calculated Lie derivatives are:

$$\begin{aligned} L_g L_f^0 h(x) = L_g h(x) &= \frac{\partial h(x)}{\partial x} g(x) \\ &= \begin{pmatrix} 0 & 1 \end{pmatrix} \begin{pmatrix} \frac{E}{L} \\ 0 \end{pmatrix} = 0 \end{aligned} \tag{10}$$

$$L_g L_f^1 h(x) = \frac{\partial [L_f h(x)]}{\partial x} g(x) = \begin{pmatrix} \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \begin{pmatrix} \frac{E}{L} \\ 0 \end{pmatrix} = \frac{E}{LC} \tag{11}$$

Since (11) is different than 0, the relative degree r of system (6) is equal to 2. The transformation of coordinates $\mathbf{x}$ to $\mathbf{z}$ is carried out by means of:

$$\mathbf{z} = \mathbf{\Phi}(\mathbf{x}) = \begin{pmatrix} z_1 \\ z_2 \end{pmatrix} = \begin{pmatrix} L_f^0 h(x) \\ L_f^{n-1} h(x) \end{pmatrix} \tag{12}$$

In order to verify if $\mathbf{\Phi}$ is a diffeomorphism, it is verified the nonsingularity of the Jacobian matrix, given by

$$\mathbf{J_\Phi} = \frac{\partial \mathbf{\Phi}(\mathbf{x})}{\partial \mathbf{x}} = \begin{pmatrix} \frac{\partial z_1}{\partial x_1} & \frac{\partial z_1}{\partial x_2} \\ \frac{\partial z_2}{\partial x_1} & \frac{\partial z_2}{\partial x_2} \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ \frac{1}{C} & -\frac{1}{RC} \end{pmatrix} \tag{13}$$

It can be shown from (13) that $\mathbf{J_\Phi}$ is nonsingular for any $\mathbf{x}$, and consequently the coordinate transformation is valid. The coordinate system $\mathbf{z}$ is expressed as:

$$\begin{aligned} z_1 &= v_C \\ z_2 &= \frac{1}{C} i_L - \frac{1}{RC} v_C \end{aligned} \tag{14}$$

The original system (6) is transformed into the linearized system in the Brunovsky normal form, as shown in the following:

$$\begin{aligned} \dot{z}_1 &= z_2 \\ \dot{z}_2 &= \alpha(x) + \beta(x)u = v \end{aligned} \tag{15}$$

where:

$$\alpha(x) = (\frac{1}{C^2 R^2} - \frac{1}{LC}) v_C - \frac{1}{C^2 R} i_L \tag{16}$$

$$\beta(x) = L_g L_f^1 h(x) = \frac{E}{LC} \tag{17}$$

Variable v is an auxiliary control law whose expression will be stated later and will define the desired tracking dynamics of the system. The control law is obtained solving (15) for u, as follows:

$$u = \frac{v - \alpha(x)}{\beta(x)} \tag{18}$$

The model of the FCMC shown in (5) considers a resistive load R of known value, but since the inverter is subject to loads of varying nature, the load current i_L will change its value depending of the load, thus causing disturbances in the output voltage of the inverter. As can be seen, the control law of Equation (18) requires the value of $\alpha(x)$, which in turn requires the measurement of i_L. A way to avoid using the current sensor is proposed in the following.

2.3. Design of the ADRC controller

Based on the ADRC approach with extended state observer, a Linear Extended State Observer (LESO) [18] is designed, making the following assumptions:

1. It is only measured the flat output $F = v_C$.
2. The nominal values of the parameters L, C, R, E are known.
3. The control input u_{av} is available.
4. The disturbance function $\alpha(x)$ is unknown, but it is considered as bounded.
5. The estimated variables of the flat output and its derivative are denoted as $F_1 = \widehat{F}$ and $F_2 = \widehat{\dot{F}}$.

6. The estimated variables of the disturbance function and its derivative are $\eta_1 = \widehat{\alpha(x)}$ and $\eta_2 = \widehat{\dot{\alpha}(x)}$.

The LESO observer is designed from (15) and is defined as follows:

$$\begin{aligned}\dot{F}_1 &= F_2 + \lambda_3(F - F_1)\\ \dot{F}_2 &= \eta_1 + \beta(x)u + \lambda_2(F - F_1)\\ \dot{\eta}_1 &= \eta_2 + \lambda_1(F - F_1)\\ \dot{\eta}_2 &= \lambda_0(F - F_1)\end{aligned} \tag{19}$$

The set of coefficients $\lambda_0, \lambda_1, \lambda_2, \lambda_3$ are constant values, and are chosen by means of a fourth order Hurwitz polynomial:

$$\begin{aligned}\lambda_0 &= \omega_n^4\\ \lambda_1 &= 4\zeta\omega_n^3\\ \lambda_2 &= 2\omega_n^2 + 4\zeta^2\omega_n^2\\ \lambda_3 &= 4\zeta\omega_n\end{aligned} \tag{20}$$

The ADRC control is designed from (18) and (19), where the estimated values of the LESO observer are adapted to the auxiliary tracking controller:

$$v = \dot{F}_2^* - k_1(F_2^* - z_2) - k_0(F_1^* - z_1) \tag{21}$$

where the tracking signals are:

$$\begin{aligned}F_1^* &= A\sin(\omega_n t)\\ F_2^* &= -A * \omega_n \cos(\omega_n t)\\ \dot{F}_2^* &= A(\omega_n)^2 \sin(\omega_n t)\end{aligned} \tag{22}$$

with $\omega_n = 2\pi f$ and $f = 60$ Hz.
The control law based on the ADRC technique is stated as follows:

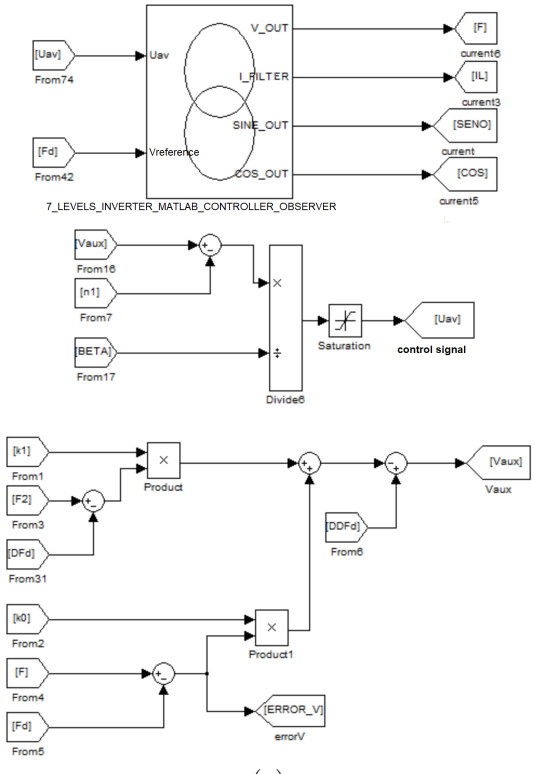
$$u = \frac{v - \eta_1}{\beta(x)} \tag{23}$$

In (22), η_1 represents the estimated value of $\alpha(x)$, i.e., $\eta_1 = \widehat{\dot{\alpha}(x)}$. The coefficients k_0, k_1 are constant values, chosen by means of a second order Hurwitz polynomial, as shown in the following:

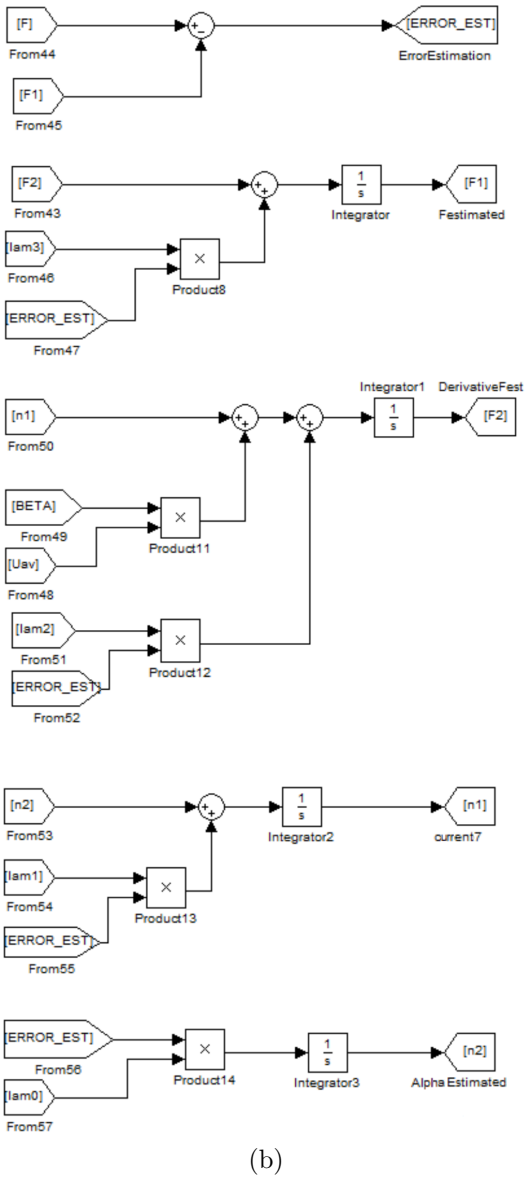
$$\begin{aligned}k_0 &= w_{nc}^2\\ k_1 &= 2\zeta_c w_{nc}\end{aligned} \tag{24}$$

3. Simulation of the system

The simulation of the system was performed using the SimCoupler module and was carried out through a cosimulation between PSIM 9.0 and MATLAB/Simulink. The controller is constructed in MATLAB/Simulink, as shown in Figure 5. On the other hand, the precharge circuit and the elements of the multilevel inverter (output filter, PS-PWM modulator and the control for load changes) are constructed in PSIM, as shown in Figure 6. Therefore, the controller processing is carried out in MATLAB/Simulink and is coupled to PSIM through the SimCoupler module; the value of the coupled control signal is called u_{av}, which is received by the PS-PWM modulator as duty cycle to perform the control action on the FCMC output.



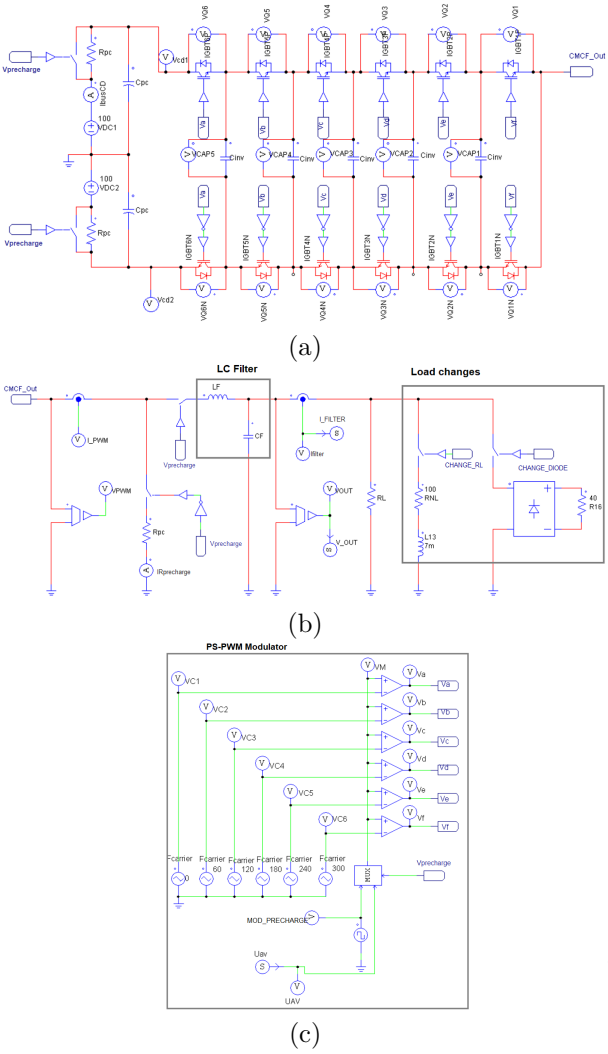
(a)



(b)

Figure 5. MATLAB/Simulink: (a) ADRC control and (b) LESO Observer.

For all passive components employed, plate nominal values were considered with a tolerance of 20 % for capacitors and of 10 % for resistors and inductors; therefore, for the multilevel converter the following values were used: $C_{CAP1...CAP5} = 10\ \mu F$; the DC bus capacitors have a value of $C_{PC} = 1000\ \mu F$. The values of the elements of the output filter are $C_F = 4.7\ \mu F$, $L_F = 7\ mH$ and $R_L = 100\ \Omega$. The voltage reference signal is equal to $Vd = A\sin(2\pi f)$, the tests were conducted for a desired amplitude $A = 80\ V$ and a frequency $f = 60\ Hz$. On the other hand, the PS-PWM modulation utilizes carriers with frequency 2.4 kHz. The value of the parameters for the LESO observer $\lambda_0,\ \lambda_1,\ \lambda_2,\ \lambda_3$ are calculated with $w_n = 30000$ and $\zeta = 0.707$. The parameters of the controller k0 and k1 are calculated with $w_{nc} = 3000$ and $\zeta_c = 0.707$. In both cases the poles are located in the left side of the complex plane, in order to guarantee the stability.



(a)

(b)

(c)

Figure 6. (a) Multilevel inverter, (b) LC filter at the output and load change control, (c) PS-PWM modulator and load changes activation.

In order to verify the robustness of the ADRC controller in the presence of sudden load changes, two types of tests were conducted: for a first test, an additional $R-L$ load, with nominal values $R_{NL1} = 80\ \Omega$ and $L_{NL} = 7\ mH$, is added at the output of the inverter, after the filter. The result of the simulation is shown in Figure 7(a), where it can be seen that when the load change occurs, the current i_L increases its value, and the LESO estimator together with the ADRC controller update the control signal u_{av}, enabling that the capacitor voltage retakes the reference trajectory again.

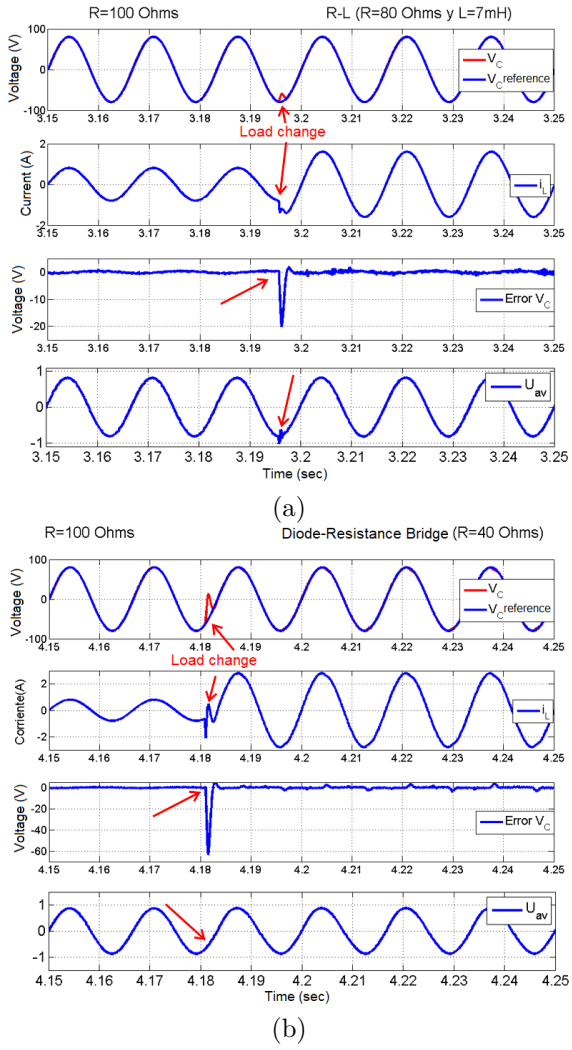


Figure 7. Simulation results: (a) With additional R – L load, (b) With additional load constituted by a bridge of diodes and a resistance.

The second test consisted in adding a nonlinear load constituted by a bridge of diodes together with a resistive load of 40 Ω. Figure 7(b) shows the result of the simulation, where it can be seen that adding the nonlinear load produces a significant transient deviation of the capacitor voltage from its sinusoidal reference, which is similarly corrected by the action of the LESO estimator and the ADRC controller.

Figure 8 shows the result of the simulation with the controller, of the behavior of the voltage in the flying capacitors during the load changes implemented in the previous tests. The precharge of the flying capacitors is carried out according to the work presented in [7], where a time interval of $t = [0 - 2]$s is proposed. In the presence of load changes, it is seen that the average voltages of the flying capacitors are maintained at their nominal values; the ripple increases, and is larger when the nonlinear load of diode + resistance is connected. To validate the effect of the controller on the output voltage v_C, two simulation tests were conducted, the first test without controller, only with the PS-PWM modulator; the result of this test can be seen in Figure 9(a). In the second test the proposed controller is utilized, and the result is shown in Figure 9(b). In this test the voltage v_C of the capacitor remains without changes or changes hardly perceptible close to the reference. At this point, and analyzing the aforementioned figures, it can be argued that the PS-PWM modulation for itself would not be capable of maintaining the output voltage.

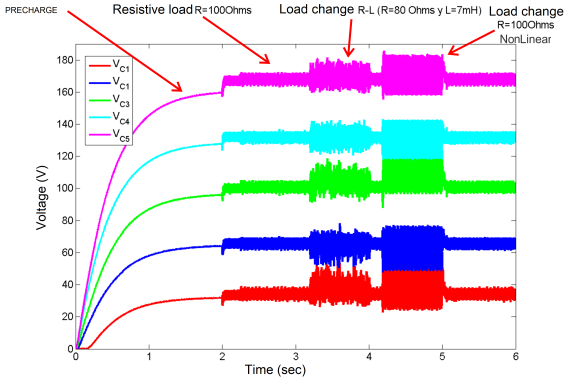


Figure 8. Simulation result of the voltages in the flying capacitors during the precharge, normal operation and load changes.

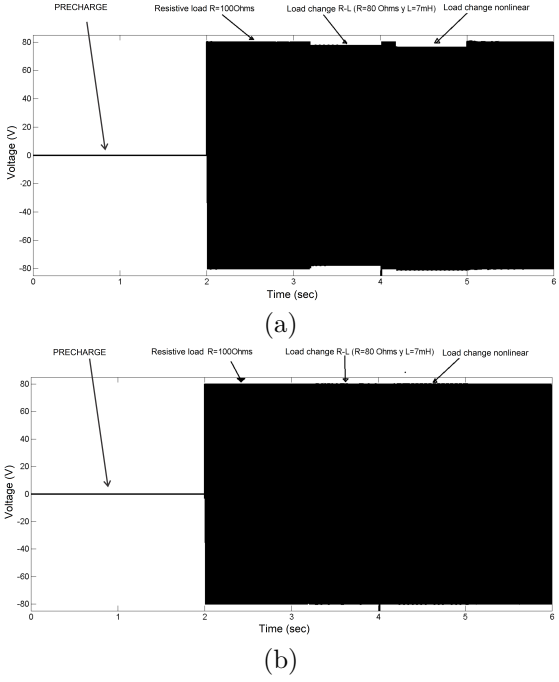


Figure 9. Simulation results for the output voltage v_C: (a) With load changes and only the PS-PWM modulator, (b) With load changes and applying the controller + LESO estimator.

4. Experimental results

In order to verify the simulation results, the implementation of the system was carried out which consisted of two main parts: the first comprises the construction of the multilevel converter prototype and of the auxiliary systems for its operation; the description of this system is shown in Figure 10.

The second part is the implementation in a FPGA of the algorithms of the ADRC controller and the PS-PWM modulator. In [19] it is recommended to follow the top-down methodology, which is very appropriate to implement algorithms in reconfigurable logic devices, and has been used with excellent performance in [14] [20–22]. In order to carry out the implementation the software Xilinx ISE 14.7 was utilized, and the coding was made in VHDL without using any high level tool based on blocks or code generation, and the internal elements of the FPGA were utilized, such as BRAM memories and embedded multipliers, to optimize the use of the device internal resources; the design which was made is shown in Figure 11. It is worth mentioning that the 32-bit simple floating point numerical representation, according to the IEEE-754 standard, was utilized for the necessary arithmetic operations, and a sampling time of 10 μs was achieved.

For evaluating the performance of the controller, two types of tests were carried out just like in simulation: open-loop and closed-loop. Linear and nonlinear load changes were made in both cases, to verify the performance of the proposed controller.

The prototype was initially tested to verify its correct operation, and the result of this test is shown in Figure 12. The output with seven levels taken before the output filter can be seen in Figure 12(a); Figures 12(b) and (c) show the sinusoidal output after the LC filter for the supplied voltage and current, respectively.

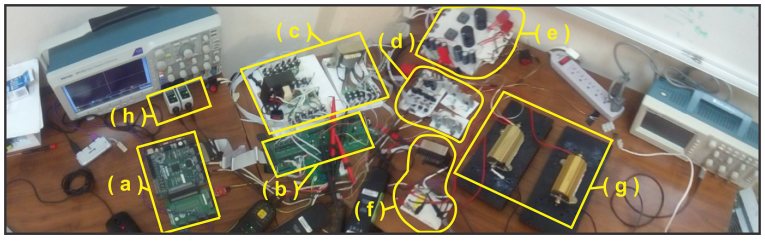


Figure 10. Developed prototype of the seven levels flying capacitor multilevel inverter: (a) Development board based on FPGA (Nexys-2), (b) Multilevel inverter, (c) Isolated sources for gate drivers and instrumentation, (d) Control of the precharge of capacitors and of the load change at the output, (e) Main DC source, (f) LC filter at the inverter output, (g) Loads at the inverter output (200 W), (h) Isolated measurement probes.

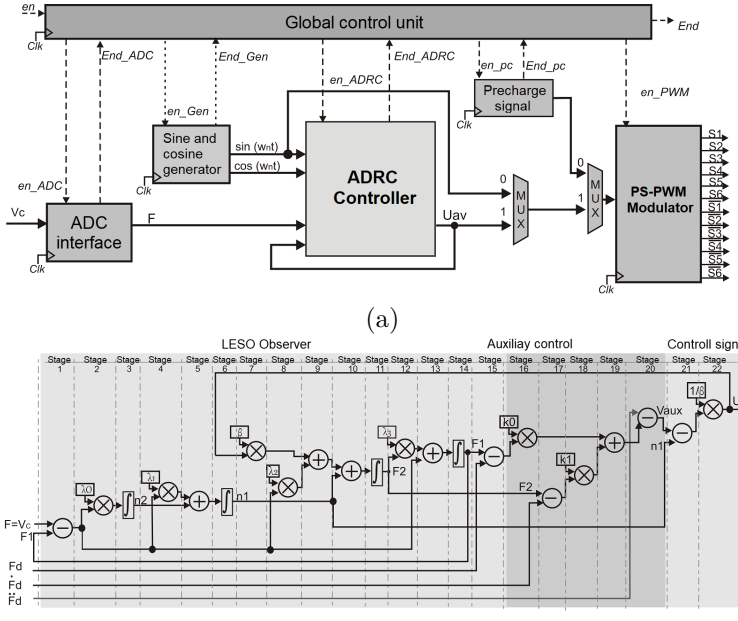


Figure 11. Implementation in the FPGA device: (a) Proposed block diagram, (b) Designed architecture for the execution of the control algorithm and LESO.

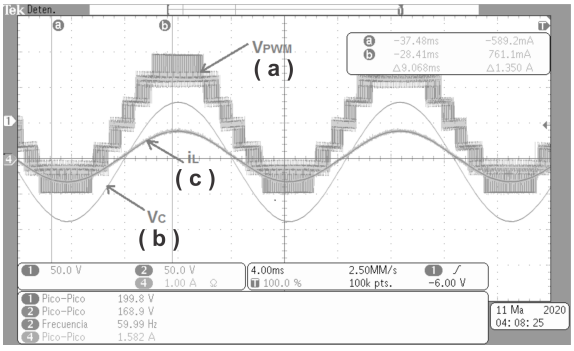


Figure 12. Shapes of the output waves obtained from the experimental prototype: (a) Multilevel output voltage of 7 levels before the LC filter (V_{PWM}), (b) Output voltage after the LC filter (V_C), (c) Current supplied to the load (i_L).

A test with a power quality meter (Hioki 3197) was carried out to validate the harmonic content of the inverter output wave; the result is shown in Figure 13, where it is observed a high quality of the output wave, both in voltage (THD_v) and current (THD_i).

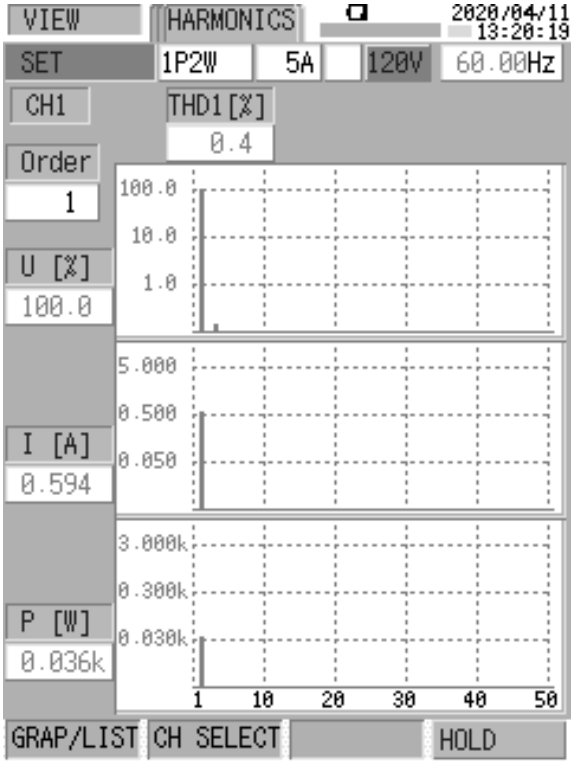


Figure 13. Result of the THD_v and THD_i measurement at the output of the multilevel inverter.

As a result of the open-loop test, Figure 14 shows the results of three aspects that are considered important: the control signal (uav), the converter output voltage (v_C) and the voltage of the capacitors ($V_{C1...C5}$). As it was previously mentioned, linear and nonlinear load changes were carried out. Figure 14(a) shows the value of the control signal with a fixed amplitude after the precharge with a value $u_{av} = 0.85$, which is equivalent to a reference value of the output voltage $V_C = 85$ V, as can be seen in Figure 14(b) when the system is subject to sudden load changes. It can be clearly observed in this figure that during transients, the voltage amplitude is affected, since it decreases. It is observed in Figure 14(c) that the balance of the capacitors is nominally maintained inside their working zone, but an increase in the ripple of each of them can be seen when load changes occur.

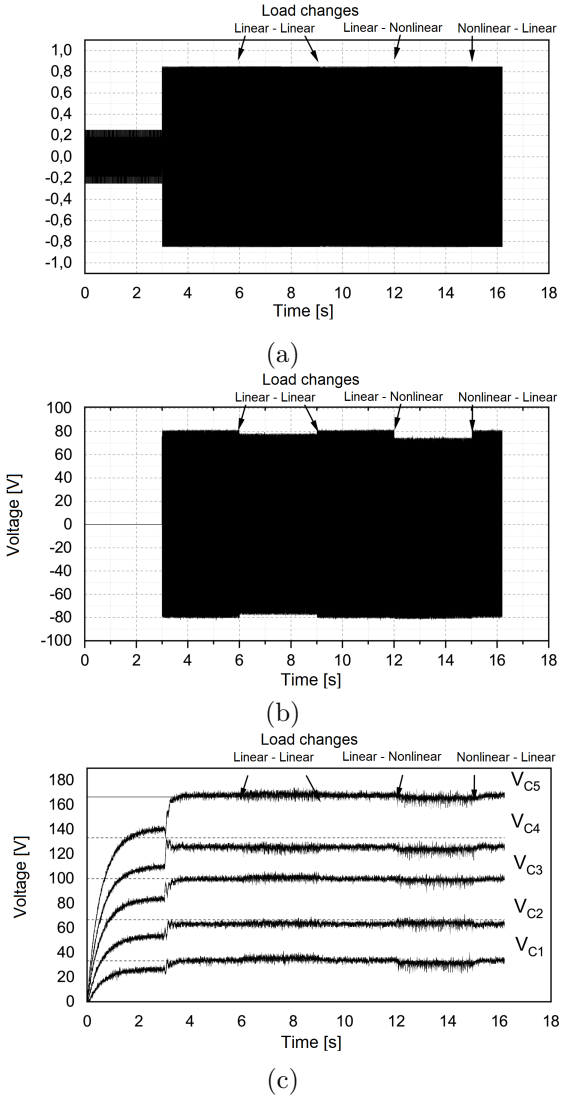


Figure 14. Plots of the experimental results obtained in open-loop in the presence of different load changes: (a) Control signal (u_{av}), (b) Inverter output voltage after the filter (V_C), (c) Voltage in the flying capacitors $V_{C1...C5}$.

The closed-loop test was carried out under the same procedure used for the open-loop test. Figure 15(a) shows the result of the control signal; after the precharge period, an initial value $u_{av} = 0.85$ is established for a reference value of $V_C = 85\ V$, and in

the same figure it can be seen the action of the controller (variable u_{av}) during the sudden connection of loads. Figure 15(b) shows that the amplitude of the output voltage does not vary when the load changes are performed. Figure 15(c) shows the voltage of the capacitors, which maintain the balance and only a high frequency increase is observed in each of them.

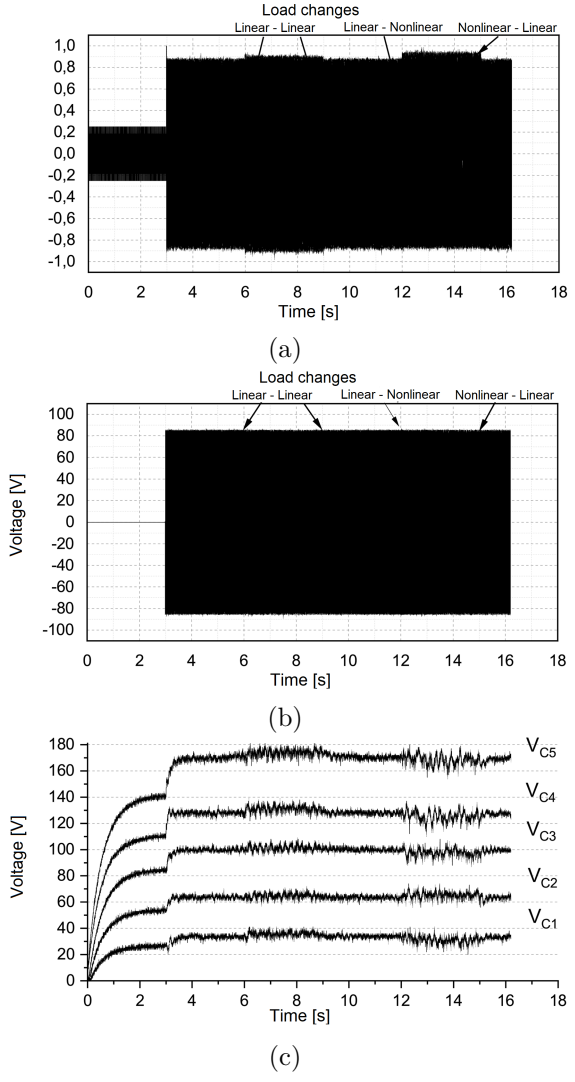


Figure 15. Plots of the experimental results obtained in closed-loop with the ADR_C controller, in the presence of different load changes: (a) Control signal (u_{av}), (b) Inverter output voltage after the filter (V_C), (c) Voltage in the flying capacitors $V_{C1...C5}$.

5. Conclusiones

In general, it is observed that reducing the complexity of the FCMC model considerably helped in other aspects such as the reduction in the computation capability necessary to process the controller, reduction of the processing time and requiring less sensors in the prototype.

On the other hand, it can be stated that it is necessary that the PS-PWM modulation maintains the balance of the 12 voltages of the flying capacitors for the ADRC control to work appropriately, i.e., so that it performs the tracking of the reference voltage, but the PS-PWM modulation is not capable of maintaining the desired output voltage at its nominal value in the presence of disturbances in the load current.

By adding the ADRC controller, the control task is carried out in an effective manner. The ADRC controller and the LESO observer effectively manage the current disturbance, and consequently the controller may be considered as robust in the presence of external disturbances produced by linear and nonlinear load changes. The voltage signal in the filter capacitor effectively tracks the imposed reference, except for transient deviations that are quickly minimized by the controller. It should be considered that in the case of unbalance of the capacitors, the ADRC control is not capable of tracking the reference voltage.

The use of the programmable logic device for implementing the system, as can be observed in experimental tests, contributed to obtaining very good results, especially in terms of speed of execution of the algorithm and attention to disturbances. It was verified that the multilevel inverters have among their main features a high quality in the output wave ($THD_v < 5$ %, as required by the IEEE-519 standard), and that the flying capacitor topology is a recommended choice among the other existing multilevel structures, since it requires only one DC source.

References

[1] D. Hart, *Electrónica de potencia.* Madrid: Pearson Education, 2001. [Online]. Available: https://bit.ly/3eJZYXH

[2] R. Haider, R. Alam, N. B. Yousuf, and K. M. Salim, "Design and construction of single phase pure sine wave inverter for photovoltaic application," in *2012 International Conference on Informatics, Electronics & Vision (ICIEV).* IEEE, may 2012. [Online]. Available: https://doi.org/10.1109/iciev.2012.6317332

[3] L. Franquelo, J. Rodríguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, "The age of multilevel converters arrives," *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28–39, jun 2008. [Online]. Available: https://doi.org/10.1109/mie.2008.923519

[4] S. A. Gonzalez, S. A. Verne, and M. I. Valla, *Multilevel Converters For Industrial Applications.* Taylor & Francis Ltd, 2017. [Online]. Available: https://bit.ly/3eN3PUc

[5] Y. Lei, C. Barth, S. Qin, W.-c. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2 kW, single-phase, 7-level, GaN inverter with an active energy buffer achieving 216 w/in^3 power density and 97.6% peak efficiency," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, mar 2016. [Online]. Available: http://doi.org/10.1109/apec.2016.7468068

[6] D. Janik, T. Kosan, P. Kamenicky, and Z. Peroutka, "Universal precharging method for dc-link and flying capacitors of four-level flying capacitor converter," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, nov 2013. [Online]. Available: https://doi.org/10.1109/IECON.2013.6700175

[7] S. Thielemans, B. Reznikov, J. Melkebeek, and A. Ruderman, "Self-precharge for single-leg odd-level multilevel converter," in *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*. Institution of Engineering and Technology, 2010. [Online]. Available: https://doi.org/10.1049/cp.2010.0142

[8] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 178–185, jan 2007. [Online]. Available: https://doi.org/10.1109/tpel.2006.886600

[9] M. Trabelsi and L. Ben-Brahim, "Experimental photovoltaic power supply based on flying capacitors multilevel inverter," in *2011 International Conference on Clean Electrical Power (ICCEP)*. IEEE, jun 2011. [Online]. Available: http://doi.org/10.1109/iccep.2011.6036314

[10] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing method for the multilevel flying capacitor converter using phase-shifted PWM," in *2012 IEEE International Conference on Power and Energy (PECon)*. IEEE, dec 2012. [Online]. Available: http://doi.org/10.1109/pecon.2012.6450221

[11] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: active control and observation of flying-capacitor voltages," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 998–1008, oct 2002. [Online]. Available: http://doi.org/10.1109/tie.2002.803200

[12] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Springer US, 2001. [Online]. Available: http://doi.org/10.1007/b100747

[13] H. Miranda, V. Cárdenas, G. Espinosa-Pérez, and D. Noriega-Pineda, "Multilevel cascade inverter with voltage and current output regulated using a passivity - based controller," in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*. IEEE, oct 2006. [Online]. Available: https://doi.org/10.1109/IAS.2006.256643

[14] J. A. Juárez-Abad, J. Linares-Flores, E. Guzman-Ramírez, and H. Sira-Ramírez, "Generalized proportional integral tracking controller for a single-phase multilevel cascade inverter: An FPGA implementation," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 256–266, feb 2014. [Online]. Available: http://doi.org/10.1109/tii.2013.2242085

[15] F. J. Chavero Ramírez, H. J. C. López Tapia, and N. V. Nava, "Estrategia de control para inversor multinivel con capacitores flotantes," *Pistas educativas*, vol. 108, no. 35, 2014. [Online]. Available: https://bit.ly/3eNaVIk

[16] M. Caris, H. Huisman, J. Duarte, and E. Lomonova, "Nonlinear and vector closed-loop control methods for flying-capacitor power converters," *International Journal of Electronics*, vol. 104, no. 8, pp. 1298–1316, mar 2017. [Online]. Available: https://doi.org/10.1080/00207217.2017.1293739

[17] D. Bhattacharyya, S. Padhee, and K. C. Pati, "Modeling of DC–DC converter using exact feedback linearization method: A discussion," *IETE Journal of Research*, vol. 65, no. 6, pp. 843–854, may 2018. [Online]. Available: https://doi.org/10.1080/03772063.2018.1454345

[18] B.-Z. Guo and Z.-L. Zhao, *Active disturbance rejection control for nonlinear systems: An introduction*. John Wiley & Sons, 2016. [Online]. Available: https://doi.org/10.1002/9781119239932

[19] H. Kaeslin, *Top-down digital VLSI design : from architectures to gate-level circuits and FPGAs*. Waltham, MA: Morgan Kaufmann, 2015. [Online]. Available: https://bit.ly/36WnwGh

[20] E. Monmasson, L. Idkhajine, I. Bahri, M-W-Naouar, and L. Charaabi, "Design methodology and FPGA-based controllers for power electronics and drive applications," in *2010 5th IEEE Conference on Industrial Electronics and Applications*. IEEE, jun 2010. [Online]. Available: https://doi.org/10.1109/ICIEA.2010.5515585

[21] J. A. Juárez-Abad, A. P. Sandoval-García, J. Linares-Flores, J. F. Guerrero-Castellanos, P. Banuelos-Sanchez, and M. A. Contreras-Ordaz,

"FPGA implementation of passivity-based control and output load algebraic estimation for transformerless multilevel active rectifier," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 4, pp. 1877–1889, apr 2019. [Online]. Available: https://doi.org/10.1109/tii.2018.2865445

[22] R. M. Lagunes, J. A. Juárez-Abad, B. A. A. López, J. L. B. Avalos, and J. L. Flores, "Control de velocidad de un motor síncrono de imanes permanentes accionado por un inversor trifásico multinivel," *Ingenius*, no. 23, pp. 97–108, dec 2019. [Online]. Available: http://doi.org/10.17163/ings.n23.2020.09